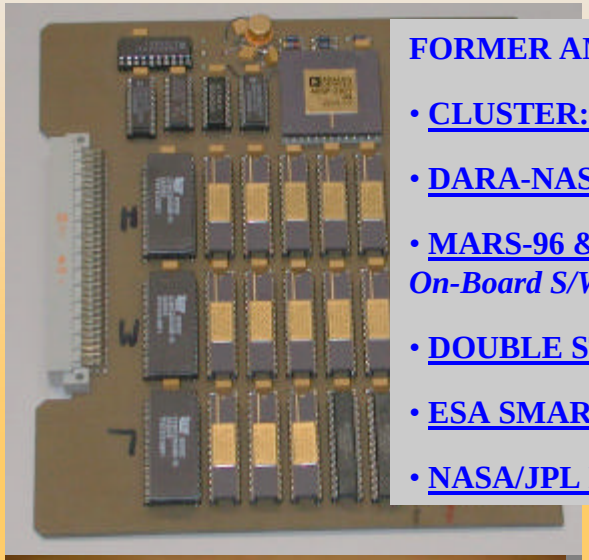
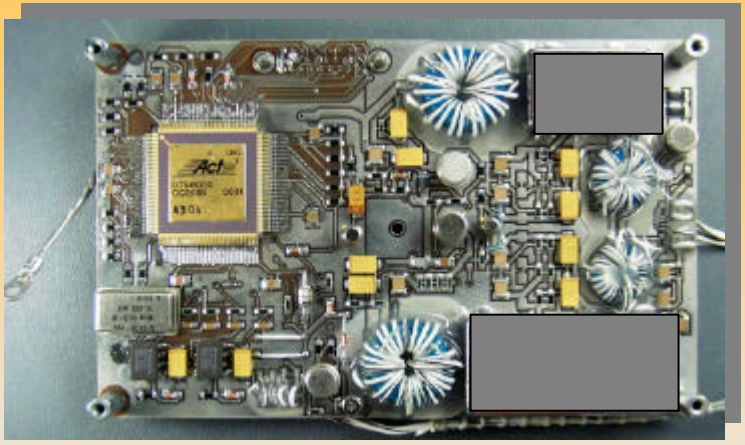
DATA HANDLING:Main DPUs inheritances



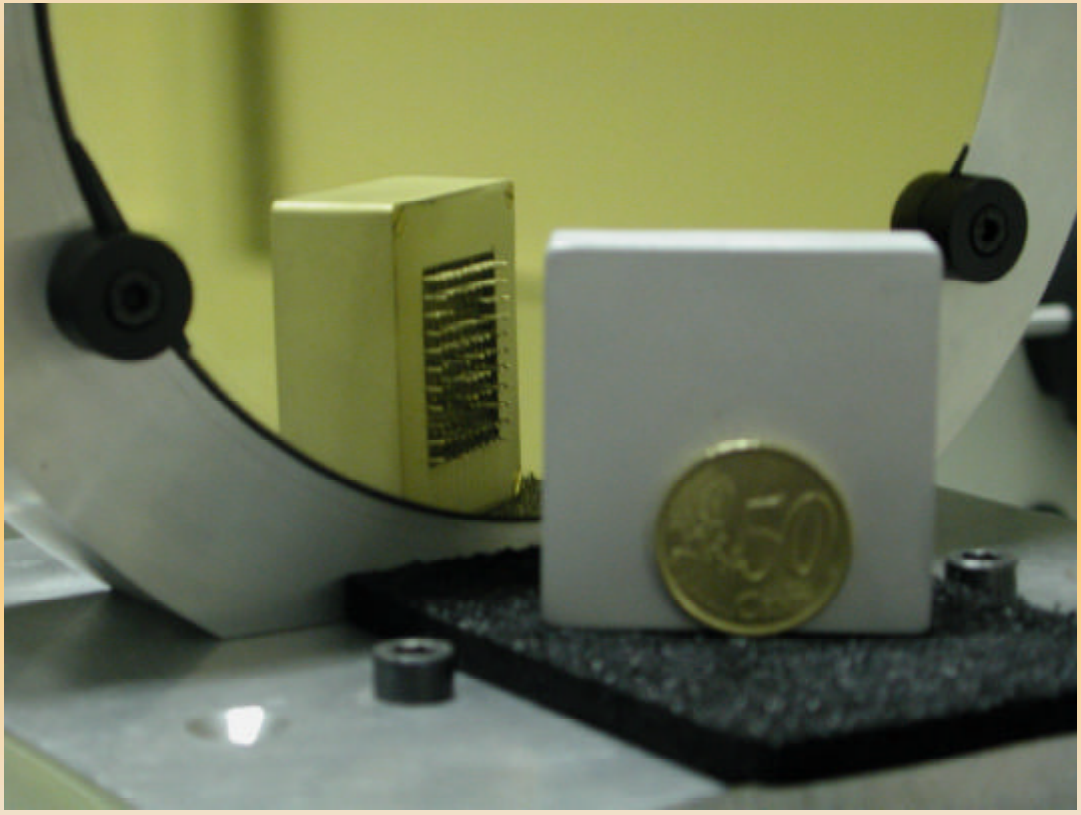
FORMER AMDL's related experiences:

- **CLUSTER: CIS-2** ***DPU Designing & On-Board S/W (MAS281)***
- **DARA-NASA EQUATOR-S: ESIC** ***- On-Board S/W (MAS281)***
- **MARS-96 & ESA MARSEXPRESS: PFS** ***- FFT DPU Design & On-Board S/W (AD21000)***
- **DOUBLE STAR** ***Composition Experiment OnBoard S/W (MAS281)***
- **ESA SMART-1: AMIE** ***Microcamera - Power supply & S/C I/F board***
- **NASA/JPL DAWN :** ***VIR On board compression S/W & GSE***



3D technologies for main DPU

PRESENT AMDL's technology: the *3*^{CUBE} uDSP based DPU

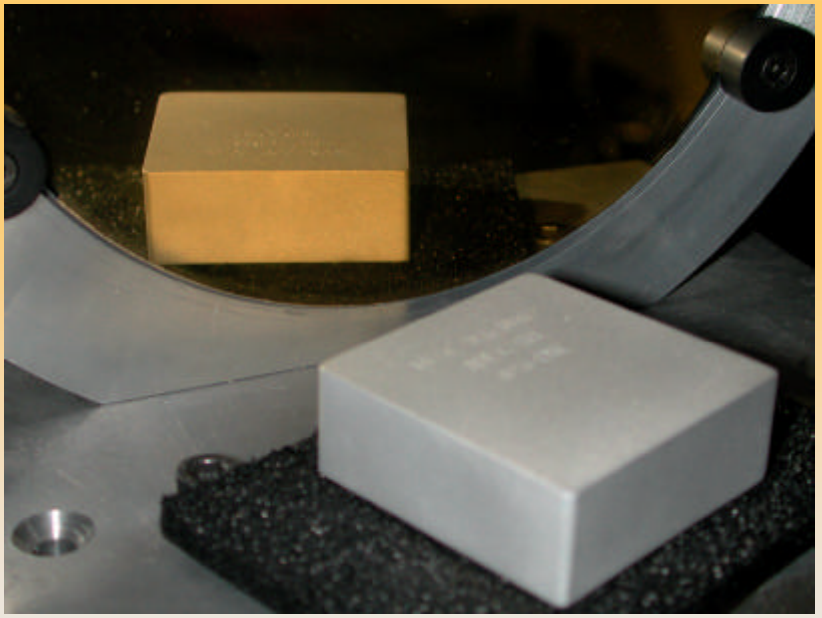


3^{Cube} Main DPU Features

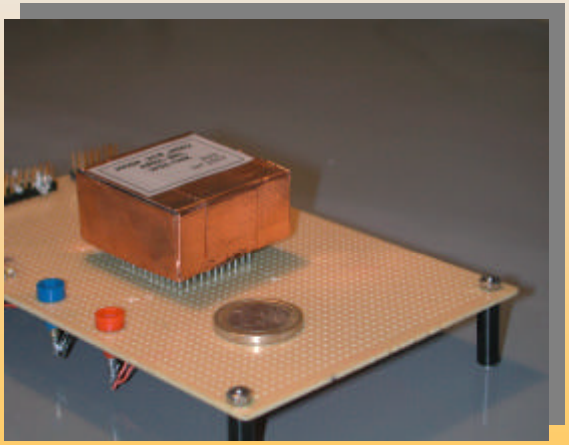
Key Features of the proposed *3^{Cube} MINI-DPU*

The *3^{Cube} MINI-DPU* has the following features:

- DSP operating up to 200 MHz (*Model 3MD-G*) or up to 120 MHz (*Model 3MD-P*)
- 4 Meg x 16 DRAM
- 1 Meg x 16 Flash Memory
- 32 Kilobyte SPI Flash Memory
- 10k gates customer programmable FPGA for user target I/F
- Universal Serial Bus (USB) interface
- Media Card MMC™ and Memory Stick MS™ interfaces
- Embedded 1149.1 JTAG Emulation
- I^2 bus I/F
- 3 x 100Mbit/s bidirectional serial buses
- +5 volt operations
- Up to 4x10 bit ADC channels
- PGA100, 0.1" pitch 100 pin interface



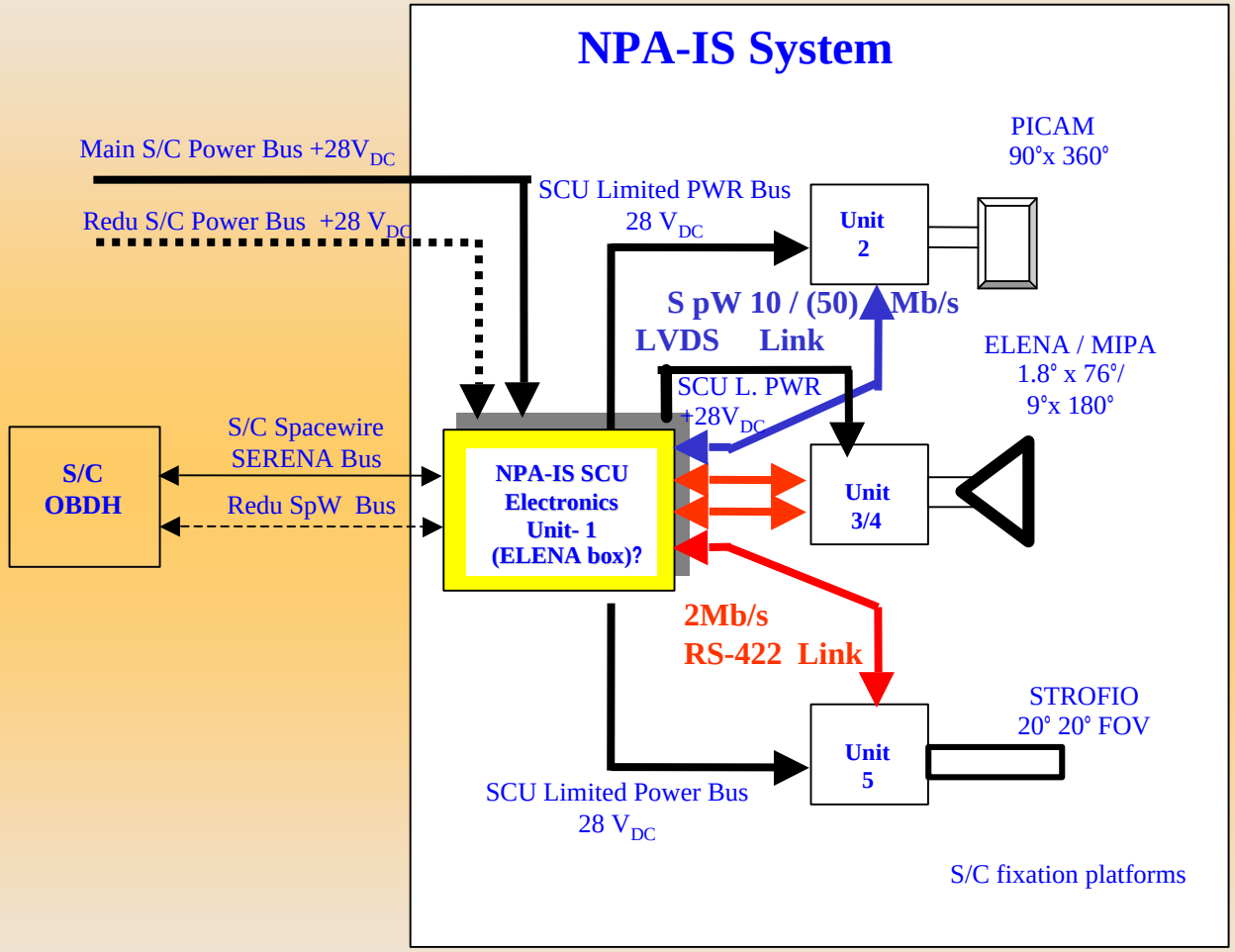
3Cube DPU lab tests gallery



(TOP) uDPU model MDSP_3CB_M002 with a thermal cover.

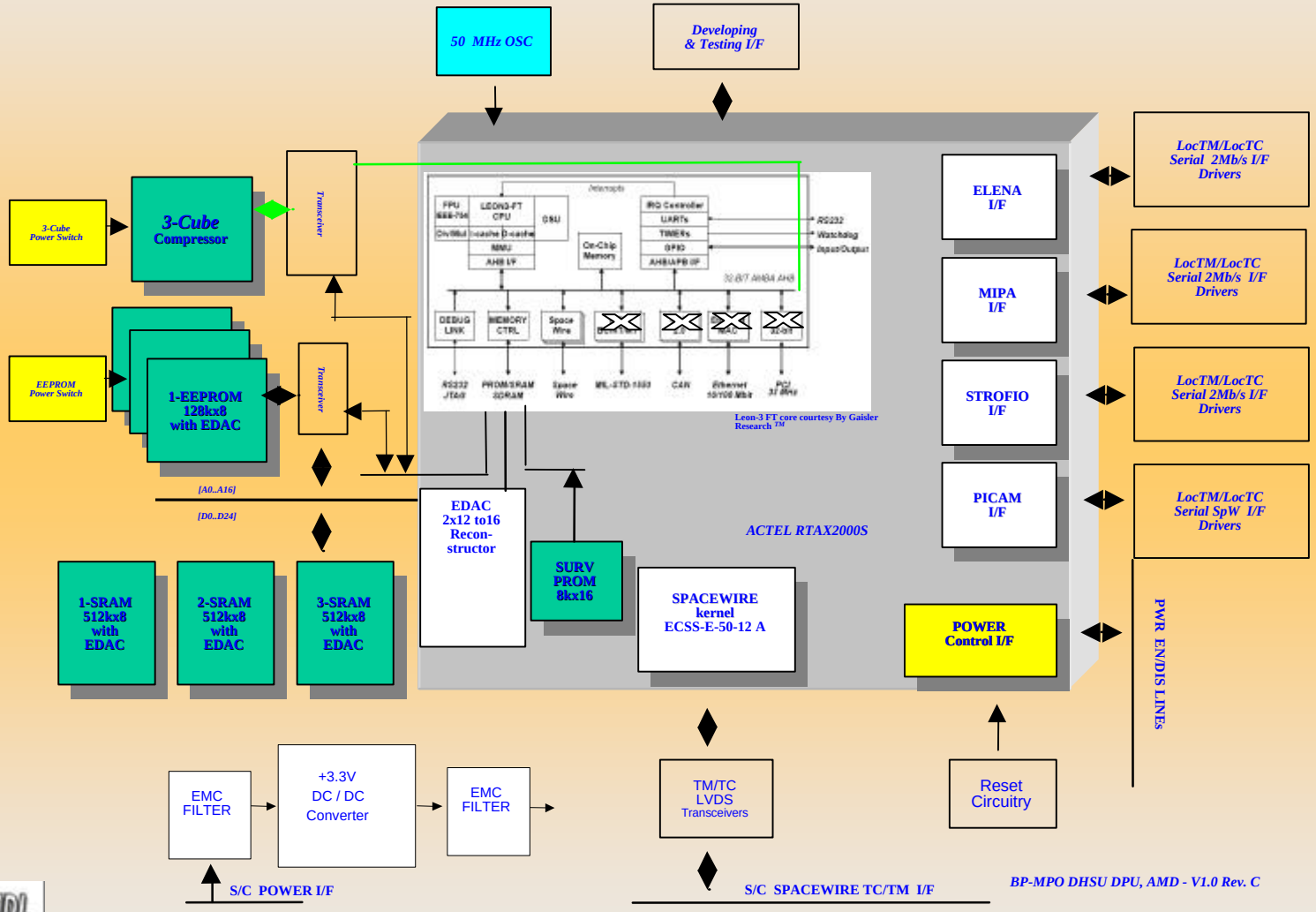
(LEFT) uDPU during memory test (500 mW on primary). (RIGHT) uDPU in stand-by (100mW on primary).

THE SERENA DHSU on BEPICOLOMBO



amdlspace@gmail.com

DHSU Block Diagram



BP-MPO DHSU DPU, AMD - V1.0 Rev. C

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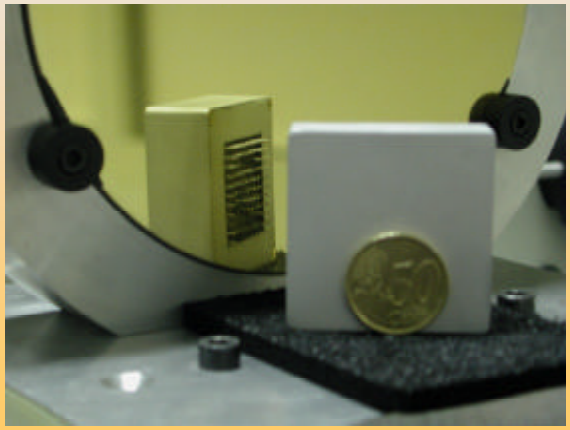
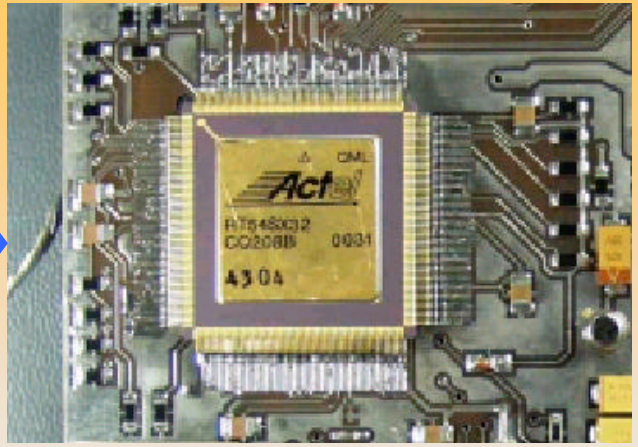
DPU Main Electronics parts

Present Generation

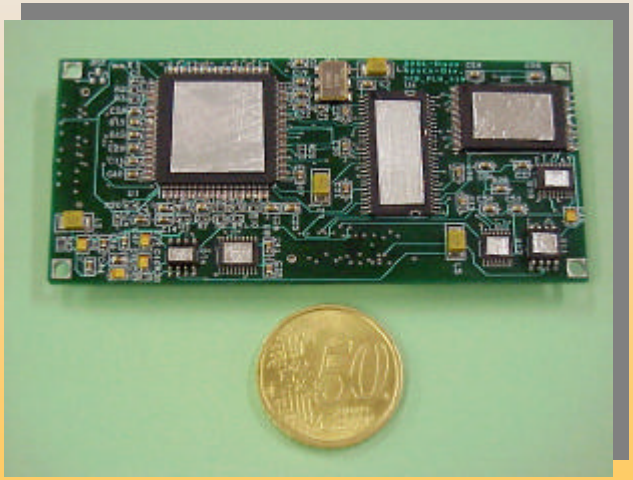


AMDL's MDSP_3CB_M003



ACTEL HI-REL RT54SX72S

NEXT GENERATION



AMDL's 3CB_PLN_010

RTAX-S RadTolerant FPGAs

- Immune to Single-Event Upsets (SEU) to LETth > 60 MeV-cm2/mg
- Single-Event Latch-Up Immunity (SEL) to LETth >104 MeV-cm2/mg
- Functional at 300 krad (Si) Total Ionizing Dose (TID) (Projected)
- SEU Rate < 10-10 Errors/Bit-Day in Worst-Case (Geosynchronous Orbit)
- Equivalent System gates up to 2,000,000

DSP Compressor facts

Compressor Core:

3^{CUBE} Planar model fully operated on Apr the 2nd 2004:

- **Used within ESA Venus's DALOMIS ITT(17946 /'03/NPLA, Sub contract DCC-LA-BN-293-04) Delivered 1st DALOMIS complete DHSU demonstrator**
- **Delivered DHSU demonstrator for an ISS High Energy application (SiRAD Sub.Con 745/2003 - 20/10/2003)**
- **Delivered DHSU 2xFM SiRAD models (Sub.Con IH.26 / 270223 - 12/12/2007)**
- **I/F'ed to a high DAQ Lab Applic. - 6xChs 30MS/s pipe and to USB 2.0 - 480Mb/s host I/F**

Weight 16.9 g!